AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method of pipelined processing of a data packet (100,315) in a processing means (700) comprising at least two processing stages (205), said data packet (100) containing information, said method comprising:~~characterised by~~

generating an intermediate data packet (315) by adding at least one of a dummy header (305) and~~/or~~ dummy tail (310) to said data packet (100) , said dummy header (305) and dummy tail (310) being capable of storing information of a communication system;

associating (510) information reference (320; 325,330) to said intermediate data packet (315), said information reference (320; 325,330) comprising information relating to the length and position of the information of said data packet (100) contained in said intermediate data packet (315);

storing said information reference (320, 325, 330) in additional register (230);

processing (520) said intermediate data packet (315) in a processing stage (205); and

~~if~~ said processing (520) of said intermediate data packet (315) results in a change of the length ~~or position~~ of said information of said data packet (100) contained in said intermediate data packet (315), ~~then~~ whereby ~~altering (530)~~ said information reference (320; 325, 330) is altered (530) in order for said information reference (320; 325, 330) to reflect said change,

wherein the change in the length of said information of said data packet (100) comprises at least one of:

adding to the length a value representing a length of a portion of the at least one of the dummy header (305) and dummy tail (310) of said intermediate data packet (315), the portion storing information of the communications system, and

subtracting from the length a value representing a portion of said intermediate data packet representing empty information after said processing.

2. (cancelled)

3. (cancelled)

4. (previously presented) The method of claim 1, the method further comprising the steps of:

determining, upon said intermediate data packet (315) exiting the last of said at least one processing stages, (540) whether any bits of said intermediate data packet (315) are superfluous; and, if any bits of said intermediate data packet (315) are superfluous, then

removing (545) said superfluous bits from said intermediate data packet (315).

5. (previously presented) The method of claim 1, the method further comprising the steps of:

removing, upon said intermediate data packet (315) exiting the last of said at least one processing stages, at least one bit from said intermediate data packet (315).

6. (previously presented) The method of claim 1, wherein said information reference (320) is included in additional information (225) associated with said intermediate data packet (315).

7. (previously presented) The method of claim 1, wherein prior to said step of processing (520) said intermediate data packet (315), said information reference (320) is stored in at least one register (230) accessible to the processing stage (205) performing said processing (520).

8. (previously presented) The method of claim 1, wherein said information reference comprises a length value (325) and an offset value (330), said length value (325) representing the length of the information contained in said intermediate data packet (315) and said offset value (330) indicating the position in said intermediate data packet (315) of the information.

9. (currently amended) A processing means for pipelined processing of a data packet (100), said processing means comprising at least one processing stage comprising a logic unit (210) and a register (220) for storing at least part of said data packet (100), said processing means ~~being characterised in that~~ comprising:

a receiver (705) is adapted to receive said data packet (100) and to generate an intermediate data packet (315) by adding at least one of a dummy header (305) and~~/or~~ a dummy tail (310) to said data packet (100), said dummy header (305) and dummy tail (310) being capable of storing information of a communications system;

at least one register (230) for storing information reference (320) associated with said intermediate data packet (315) is accessible to said logic unit (210), said information reference (320) comprising information relating to the length and position of the information of the data packet (100) contained in said intermediate data packet (315); ~~and~~

at least one of at said at least one logic units (210) is adapted to operate upon said information reference (320); and

a processing stage (205) for processing said intermediate data packet (315), wherein the length of the information of the data packet (100) contained in said intermediate data packet (315) changes upon processing said intermediate data packet (315) in said processing stage (205), whereby said information reference (320,325,330) is altered (530) in order for said information reference (320,325,330) to reflect said change,

wherein the change in the length of said information of said data packet (110) comprises at least one of:

adding to the length a value representing a length of the portion of the at least one of the dummy header (305) and dummy tail (310) of said intermediate data packet (315), the portion storing information of the communications system, and

subtracting from the length a value representing a portion of said intermediate data packet (315) comprising empty information after said processing.

10. (cancelled)

11. (previously presented) The processing means of claim 9, wherein said receiver (715) for adding comprises a buffer (720) and a shifter (725).

12. (previously presented) The processing means of claim 9, the processing means further comprising means (730) for removing at least one bit from said intermediate data packet (315).

13. (previously presented) The processing means of claim 9, wherein means (730) for removing comprises a shifter (735) and a buffer (740).

14. (previously presented) The processing means of claim 11, wherein said shifter (725,735) is a barrel shifter.

15. (previously presented) The processing means (700) of claim 9, wherein said at least one register (230) for storing information reference (230) is located in said processing stage (205).

16. (previously presented) The processing means (700) of claim 9, wherein said at least one register (230) for storing information reference comprises one register (230) for storing a length value (325) and another register (230) for storing an offset value (330).

17. (original) An integrated circuit, characterised by a processing means (700) according to claim 9.

18. (original) A computer unit characterised by an integrated circuit according to claim 9.

19. (currently amended) A pipelined processor for processing a data packet (100), comprising:

a register (100) for storing at least part of the data packet (100);

at least one additional register (230) for storing an information reference (320) for association with an intermediate data packet (315) ;

a logic unit (210) performing the steps of:

receiving the data packet (100);

generating the intermediate data packet (315) by adding at least one of a dummy header (305) and~~/or~~ dummy tail (310) to the data packet (100);

associating (510) information reference (320; 325,330) to the intermediate data packet (315), the information reference (320; 325,330) comprising information relating to the length and position of the information of the data packet (100) contained in the intermediate data packet (315);

storing the information reference (320, 325, 330) in the at least one additional register (230);

processing (520) the intermediate data packet (315) in a processing stage (205); and

~~if~~ said processing (520) of the intermediate data packet (315) results in a change of the length ~~or position~~ of said information of the data packet (100) contained in the intermediate data packet (315), then altering (530) the information reference (320; 325,330) in order for the information reference (320; 325, 330) to reflect the change,

wherein the change in the length of said information of said data packet (100) comprises at least one of:

adding to the length a value representing a length of a portion of the at least one of the dummy header (305) and dummy tail (310) of said intermediate data packet (315), the portion storing information of the communications system, and

subtracting from the length a value representing a portion of said intermediate data packet (315) comprising empty information after said processing.

20. (new) The method of claim 1, wherein said processing (520) of said intermediate data packet (315) further results in a change of the position of said information of said data packet (100) contained in said intermediate data packet (315), whereby said information reference (320; 325,330) is altered (530) in order for said information reference (320; 325, 330) to reflect said change, and wherein the change in the position of said information of said data packet (100) comprises at least one of:

subtracting from the position a value representing a length of the portion of the dummy header (305) of said intermediate data packet (315) containing the information of the communications system, and

adding to the position a value representing a portion of said intermediate data packet representing empty information after said processing.

21. (new) The processing means of claim 9, wherein the processing stage (205) for processing said intermediate data packet (315), is configured to process said intermediate data packet (315) resulting in a change of the position of said information of said data packet (100) contained in said intermediate data packet (315), whereby said information reference (320; 325,330) is altered (530) in order for said information reference (320; 325, 330) to reflect said change, and wherein the change in the position of said information of said data packet (100) comprises at least one of:

subtracting from the position a value representing a length of the portion of the dummy header (305) of said intermediate data packet (315) containing the information of the communications system, and

adding to the position a value representing a portion of said intermediate data packet representing empty information after said processing.

22. (new) The pipelined processor of claim 19, wherein the processing stage (205) for processing said intermediate data packet (315), is configured to process said intermediate data packet (315) resulting in a change of the position of said information of said data packet (100) contained in said intermediate data packet (315), whereby said information reference (320; 325,330) is altered (530) in order for said information reference (320; 325, 330) to reflect said change, and wherein the change in the position of said information of said data packet (100) comprises at least one of:

subtracting from the position a value representing a length of the portion of the dummy header (305) of said intermediate data packet (315) containing the information of the communications system, and

adding to the position a value representing a portion of said intermediate data packet representing empty information after said processing.